WHAT IS CLAIMED IS:

1. A digital signal processing device for processing a video signal and an audio signal to each of which time information for synchronization has been added and outputting the processed signals, comprising:

a clock generator for generating a reference clock without referring to said time information for synchronization;

a video signal processing unit which is made operative by said reference clock, executes a decoding process of the inputted video signal, and performs synchronization, on a frame unit basis, of input side frame reference timing which is obtained on the basis of said time information for synchronization and frame reference timing for output which is obtained by frequency dividing said reference clock; and

an audio signal processing unit which is made operative by said reference clock and executes a sampling transformation in a manner such that a decoding process of the audio signal is executed, a difference between periods of said input side frame reference timing and said frame reference timing for output is detected, and the number of samples is corrected in accordance with the detected period difference.

2. A device according to claim 1, wherein

said video signal processing unit operates in a manner such that in the case where said frame refer-

ence timing for output is earlier than said input side frame reference timing, a frame which has already been outputted is repetitively outputted and in the case where said frame reference timing for output is later than said input side frame reference timing, the frames are decimated and outputted, and

said audio signal processing unit operates in a manner such that in the case where said frame reference timing for output is earlier than said input side frame reference timing, a phase difference period is obtained from said input side frame reference timing and said frame reference timing for output, the number of samples of the audio signal corresponding to said phase difference period is subtracted from the number of samples of the input audio signal included in one frame period in which the input side frame reference timing is used as a reference, and by executing an enlarging or reducing process to the audio signal of the subtracted number of samples, the audio signal synchronized with said frame reference timing for output is outputted, and in the case where said frame reference timing for output is later than said input side frame reference timing, the phase difference period is obtained from said input side frame reference timing and said frame reference timing for output, the number of samples of the audio signal corresponding to said phase difference period is added to the number of samples of the input audio signal included in one frame

period in which the input side frame reference timing is used as a reference, and by executing the enlarging or reducing process to the audio signal of the added number of samples, the audio signal synchronized with said frame reference timing for output is outputted.

3. A digital signal processing device for inputting a digital signal to which a time reference signal has been added, processing said signal, and obtaining a reproduction signal of a video image and an audio sound, comprising:

a clock signal generator for generating a clock signal asynchronized with said time reference signal;

a frequency dividing unit for frequency dividing the clock signal which is outputted from said clock signal generator and generating a frame sync signal for output, a clock enable signal for an input process, and a clock enable signal according to an audio operating mode;

a digital interface processor for separating a compressed video signal, an audio signal, auxiliary information, and an input side frame sync signal from the inputted digital signal in accordance with the clock enable signal for the input process which is outputted from said frequency dividing unit and outputting them;

a video signal processing unit for inputting the compressed video signal and the input side frame

sync signal which are outputted from said digital interface processor and the clock enable signal for the input process and the frame sync signal which are outputted from said frequency dividing unit, obtaining a video signal by performing a decoding process, and executing a synchronizing process to said frame sync signal for output which is outputted from said frequency dividing unit and said input signal; and

an audio signal processing unit for inputting audio information and the frame sync signal which are outputted from said digital interface processor, the clock enable signal for the input process and the input side frame sync signal which are outputted from said frequency dividing unit, the clock enable signal according to said audio operating mode, and said frame sync signal for output which is outputted from said frequency dividing unit, obtaining the audio signal by performing a signal process, and outputting the audio signal by the clock enable signal according to said audio operating mode which is outputted from said frequency dividing unit.

4. A device according to claim 3, wherein

said video signal processing unit operates in a manner such that in the case where said frame sync signal for output is earlier than said input side frame sync signal, a frame which has already been outputted is repetitively outputted and in the case where said frame sync signal for output is later than said input

side frame sync signal, the frames are decimated and outputted, and

said audio signal processing unit operates in a manner such that in the case where said frame sync signal for output is earlier than said input side frame sync signal, a phase difference period is obtained from said input side frame sync signal and said frame sync signal for output, the number of samples of the audio signal corresponding to said phase difference period is subtracted from the number of samples of the input audio signal included in one frame period in which said input side frame sync signal is used as a reference, and by executing an enlarging or reducing process to the audio signal of the subtracted number of samples, the audio signal synchronized with said frame sync signal for output is outputted, and in the case where said frame sync signal for output is later than said input side frame sync signal, the phase difference period is obtained from said input side frame sync signal and said frame sync signal for output, the number of samples of the audio signal corresponding to said phase difference period is added to the number of samples of the input audio signal included in one frame period in which the input side frame sync signal is used as a reference, and by executing the enlarging or reducing process to the audio signal of the added number of samples, the audio signal synchronized with said frame sync signal for output is outputted.

5. A device according to claim 1, wherein said video signal and audio signal to which said time information for synchronization has been added are signals which were transmitted and inputted in a format of an IEEE1394 standard.

6. A device according to claim 3, wherein the digital signal to which said time reference signal has been added is a signal which was transmitted and inputted in a format of an IEEE1394 standard.

7. A DV decoder for processing an audio signal to which time information for synchronization has been added by a reference clock outputted from a clock generator for generating the reference clock without referring to said time information for synchronization and outputting the processed audio signal, comprising:

a frequency dividing unit for forming a frame sync signal for output on the basis of said reference clock; and

an audio signal processing unit for executing a sampling transforming process of said inputted audio signal by setting the number of samples of one frame period in which said frame sync signal for output is used as a reference to the number of samples of one frame.

8. A DV decoder for processing a video signal and an audio signal to each of which time information for synchronization has been added by a reference clock outputted from a clock generator for generating the

reference clock without referring to said time information for synchronization and outputting the processed video and audio signals, comprising:

a frequency dividing unit for forming a frame sync signal for output on the basis of said reference clock;

a video signal processing unit for processing said inputted video signal and outputting the video signal synchronized with said frame sync signal for output; and

an audio signal processing unit for executing a sampling transforming process of said inputted audio signal in a manner such that the number of samples of one frame period in which said frame sync signal for output is used as a reference is equal to the predetermined number of samples.

9. A DV decoder for inputting a video signal, an audio signal, auxiliary information, and an input side frame sync signal, processing said video signal and said audio signal by a reference clock which is asynchronous with said input side frame sync signal and is outputted from a clock generator, and outputting the processed video and audio signals, comprising:

a frequency dividing unit for forming a frame sync signal for output on the basis of said reference clock;

a video processing unit for frame synchronously processing said inputted video signal and

forming the video signal synchronized with said frame sync signal for output; and

an audio processing unit for comparing said input side frame sync signal with said frame sync signal for output, setting the number of samples of one frame period which is obtained by subtracting or adding the number of samples corresponding to a difference between said input side frame sync signal and said frame sync signal for output from/to AF_SIZE obtained from said auxiliary information to the number of samples of one frame period, and executing a sampling transforming process of said inputted audio signal.

10. A DV decoder for inputting a video signal, an audio signal, auxiliary information, and an input side frame sync signal of a DV format, processing said video signal and said audio signal by a reference clock which is asynchronous with said input side frame sync signal and is outputted from a clock generator, and outputting the processed video and audio signals, comprising:

a separating unit for separating said inputted video signal and audio signal;

a first frequency dividing unit for forming an enable signal for an input process on the basis of said reference clock;

a second frequency dividing unit for forming an enable signal for an audio signal process on the basis of said reference clock and sampling frequency information of said auxiliary information;

a third frequency dividing unit for forming a frame sync signal for output on the basis of said reference clock;

a video signal processing unit for frame synchronously processing the video signal separated by said separating unit and outputting the video signal synchronized with said frame sync signal for output;

an audio signal processing unit for writing the audio signal separated by said separating unit into a memory in response to said enable signal for the input process and reading out said audio signal;

a comparing unit for comparing said input side frame sync signal with said frame sync signal for output, adding or subtracting the number of samples of a period corresponding to a difference between said input side frame sync signal and said frame sync signal for output to/from AF_SIZE as said auxiliary information of said audio signal, and calculating the number of samples corresponding to one frame period of said frame sync signal for output; and

a sampling transform processor for executing a transforming process of the number of samples to said audio signal outputted from said audio signal processing unit by performing an enlarging or reducing process on the basis of a comparison result of said comparing unit and outputting the audio signal in response to said enable signal for the audio signal process.

11. A DV decoder for processing a video signal

and an audio signal to each of which time information for synchronization has been added by a reference clock outputted from a clock generator for generating the reference clock without referring to said time information for synchronization and outputting the processed video and audio signals, comprising:

a frequency dividing unit for forming a frame sync signal for output and a clock enable signal for an input process on the basis of said reference clock;

an input processing unit for separating and outputting the video signal, the audio signal, and an input side frame sync signal from the inputted video signal and audio signal in response to the clock enable signal for the input process which is outputted from said frequency dividing unit;

a video processing unit for processing the video signal which is outputted from said input processing unit and forming the video signal synchronized with said frame sync signal for output; and

an audio signal processing unit for executing a sampling transforming process to the audio signal which is outputted from said input processing unit so that the number of samples of one frame period in which said frame sync signal for output is used as a reference is equal to the predetermined number of samples.

12. A DV decoder for processing a compressed video signal and an audio signal to each of which time information for synchronization has been added by a

reference clock outputted from a clock generator for generating the reference clock without referring to said time information for synchronization and outputting the processed video and audio signals, comprising:

a frequency dividing unit for forming a frame sync signal for output and a clock enable signal for an input process on the basis of said reference clock;

an input processing unit for separating and outputting the compressed video signal, the audio signal, auxiliary information, and an input side frame sync signal from the inputted compressed video signal and audio signal in response to the clock enable signal for the input process which is outputted from said frequency dividing unit;

a video processing unit for decoding the compressed video signal which is outputted from said input processing unit in response to said clock enable signal for the input process and forming the video signal which is frame synchronized with said frame sync signal for output; and

an audio processing unit for executing a sampling transforming process to the audio signal which is outputted from said input processing unit by setting the number of samples obtained by adding or subtracting the number of samples corresponding to a difference between said input side frame sync signal and said frame sync signal for output to/from AF_SIZE obtained from said auxiliary information to the number of

samples of one frame period.

13. A device according to claim 3, wherein

said frequency dividing unit has a first frequency dividing unit for forming a clock enable signal for an input process on the basis of said reference clock, a second frequency dividing unit for forming a clock enable signal for an audio signal process on the basis of said reference clock and sampling frequency information included in said auxiliary information, and a third frequency dividing unit for forming a frame sync signal for output on the basis of said reference clock,

said input processing unit has an IEEE interface unit for separating and outputting the input side frame sync signal in response to said clock enable signal for the input process which is outputted from said first frequency dividing unit and a signal separating unit for separating the audio signal and the compressed video signal from the signal outputted from said IEEE interface unit,

said video processing unit has a video processor for decoding the compressed video signal which is outputted from said signal separating unit and a video synchronizer for performing a frame synchronizing process to the video signal outputted from said video processor and forming the video signal synchronized with said frame sync signal for output, and

said audio processing unit has a comparing

unit for comparing said input side frame sync signal with said frame sync signal for output, adding or subtracting the number of samples corresponding to a difference between said input side frame sync signal and said frame sync signal for output to/from AF_SIZE obtained from said auxiliary information, and calculating the number of samples of one frame period in which said frame sync signal for output is used as a reference and a sampling transform processor for executing a sampling transforming process to said audio signal by performing an enlarging or reducing process by setting the number of samples calculated by said comparing unit to the number of samples of one frame period.

14. A decoder according to claim 7, wherein the inputted audio signal is a signal in an unlocked mode in a DV standard, and said audio processing unit transforms the number of samples into the number of samples which has been predetermined in a locked mode in the DV standard.

15. A decoder according to claim 8, wherein the inputted audio signal is a signal in an unlocked mode in a DV standard, and said audio processing unit transforms the number of samples into the number of samples which has been predetermined in a locked mode in the DV standard.

16. A decoder according to claim 10, wherein the inputted audio signal is a signal in an unlocked mode

in a DV standard, and said sampling transform processor transforms the number of samples into the number of samples which has been predetermined in a locked mode in the DV standard.

17. A recording device comprising:

the DV decoder according to claim 7;

an MPEG compressing unit for compressing the video signal and the audio signal outputted from said DV decoder by MPEG compression and forming compressed data; and

a recording unit for recording the compressed data outputted from said MPEG compressing unit.

18. A recording device comprising:

the DV decoder according to claim 8;

an MPEG compressing unit for compressing the video signal and the audio signal outputted from said DV decoder by MPEG compression and forming compressed data; and

a recording unit for recording the compressed data outputted from said MPEG compressing unit.

19. A device according to claim 17, wherein said MPEG compressing unit executes a compressing process by the reference clock outputted from said clock generator.

20. A device according to claim 18, wherein said MPEG compressing unit executes a compressing process by the reference clock outputted from said clock generator.

21. A signal processing method in a DV decoder for processing an inputted video signal and an inputted audio signal by a reference clock which is asynchronous with time information for synchronization added to said video signal and said audio signal, comprising the steps of:

inputting the video signal and the audio signal;

synchronizing said inputted video signal on a frame unit basis in response to said reference clock;

outputting the video signal which was synchronized on said frame unit basis;

sampling transforming said inputted audio signal in response to said reference clock; and

outputting the audio signal which was sampling transformed on a frame unit basis different from said time information for synchronization.